Confirmation No. 8636

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	DE GROOT, *et al.*	Examiner:	Ekamin, A.
Serial No.:	10/532,294	Group Art Unit:	2116
Filed:	April 21, 2005	Docket No.:	NL021047US
Title:	DEVICE FOR EXCHANGING DATA SIGNALS BETWEEN TWO CLOCK DOMAINS		

APPEAL BRIEF

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 21, 2007 and in response to the rejections of claims 1-10 as set forth in the Final Office Action dated September 18, 2007, and in further response to the Advisory Action dated November 6, 2007.

Please charge Deposit Account number 50-0996 (NXPS.329PA) $510.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 016932/0590 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application have been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1- 10 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

All amendments have been entered.

V. Summary of Claimed Subject Matter

Appellant's recited invention relates to a device for transferring data signals between different clock domains.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a device (*see, e.g.,* device 30 shown in Fig. 3 and device 50 shown in Fig. 5, along with accompanying discussions) for exchanging data signals between a first clock domain (*see, e.g.,* first clock domain 11 in Figs. 1 and 3-6, along with accompanying discussions) and a second clock domain (*see, e.g.,* second clock domain 12 in Figs. 1 and 3-6, along with accompanying discussions), characterized in that the device comprises a serial memory element in which successive data elements are shifted in order from one memory location to a next successive memory location (*see, e.g.,* serial memory element 32 in Fig. 3

and serial memory element 64 in Fig. 4, along with accompanying discussions), and a parallel memory element coupled to the serial memory element (*see, e.g.,* parallel memory element 38 in Fig. 3 and parallel memory element 52 in Fig. 4, along with accompanying discussions), the serial memory element comprising at least one memory location more for the data signals than the parallel memory element (*see, e.g.,* paragraphs [0019] and [0026]).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The only ground of rejection remaining to be reviewed on appeal is as follows:

A. Claims 1-10 stand rejected under 35 U.S.C. § 102(e) over Kanazashi (U.S. Patent No. 7,148,826).

VII. Argument

A. The rejection of claims 1-10 under 35 U.S.C. § 102(e) over Kanazashi (U.S. Patent No. 7,148,826) should be reversed.

As set forth below, Appellant submits that the claimed invention is allowable over the cited reference because the cited reference fails to teach all of Appellant's claim elements, which include exchanging data signals between two clock domains using both a serial memory element and a parallel memory element coupled to the parallel memory element, the serial memory element having at least one memory location more than the parallel memory

element. Appellant submits that the Examiner has not demonstrated that Kanazashi discloses any of the following: (1) both a serial element and a parallel memory element coupled to a serial memory element; (2) exchange of data signals between clock domains; (3) operation of serial and parallel memory elements in different clock domains; or (4) a parallel memory element arranged for writing data signals. Because Kanazashi does not teach all the elements recited in Appellant's claims, Appellant requests that the Board reverse the § 102(e) rejection.

1. Kanazashi does not disclose a parallel memory element coupled to a serial memory element.

As discussed, Appellant's claims recite both a serial memory element and a parallel memory element for exchanging data between clock domains. While the Examiner has identified the shift register (14) in Kanazashi's Figure 5 as corresponding to the claimed serial memory, the Examiner has failed to identify anything corresponding to the claimed parallel memory element. In the Final Office Action, the Examiner cited only to Kanazashi's Figure 5 generally as disclosing a parallel memory element without providing any specificity as to what portions supported the alleged correspondence. In the Response to the Final Office Action, Appellant discussed the insufficiency of the rejection, and pointed out that no element in Kanazashi's Figure 5 corresponded to the recited parallel memory element. Appellant further discussed why the shift register shown in Kanazashi's Figure 5 could not properly be interpreted as also reading on the recited parallel memory element. As Appellant explained in the Response, the claimed invention recites that the serial memory element has at least one more memory location than the parallel memory element. As such, any assertion that Kanazashi's shift register (14) corresponds to both the serial memory element and the parallel memory element would necessarily fail to correspond to the claimed invention because they would by definition have the same number of memory locations.

In the Advisory Action mailed November 6, 2007, the Examiner effectively acknowledged that the final rejection was insufficient and wrong by attempting to identify a new and different rationale for asserting the Kanazashi reference. The Examiner now alleges that the NAND gates (21-23) in Kanazashi's Figure 5 correspond to the recited parallel memory element, baldly stating without further explanation that these gates "resemble a 3-bit

parallel memory." Because such rationale was first presented in the Advisory Action after the final rejection, the new grounds are not on appeal. Notwithstanding, Appellant finds no teaching in Kanazashi that the NAND gates shown in Figure 5 could possibly function as a parallel memory element as recited in Appellant's claims. Kanazashi teaches that input data is supplied to a shift register (14) and that the input data stored in the shift register is outputted to the data bus (A3, A2, A1, A0) through NAND gates (21-23). *See, e.g.,* Col. 4:53-67. The disclosed circuit thus converts the input serial data into parallel data that can be output to a data bus. *See, e.g.,* Col. 3:57-62. The Examiner identified the shift register (14) as the claimed serial memory element, and now identifies the NAND gates (21-23) as the claimed parallel memory element. Appellant finds no disclosure in Kanazashi that the NAND gates perform a memory or storage function or any other function besides serving as logic gates that pass through output signals based on input signals.

Appellant further submits that the Examiner's interpretation of Kanazashi's NAND gates as resembling a parallel memory element is inconsistent with the ordinary meaning of that term. According to M.P.E.P. § 2111.01, during examination the USPTO must give claims their broadest reasonable interpretation in light of the specification, meaning that the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification. The ordinary and customary meaning of a term may be evidenced by a variety of sources, including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *See Phillips v. AWH Corp.*, 415 F.3d at 1314 (Fed. Cir. 2005).

One of ordinary skill understands that memory in the context of computing is something that preserves data for later retrieval. This is consistent with the ordinary meaning of the term "memory" as applied to computer science as evidenced by any of a variety of current dictionary sources. *See, e.g.*, Merriam-Webster's Online dictionary entry <http://www.m-w.com/dictionary/memory>. Appellant therefore submits that Examiner's assertion that Kanazashi's NAND gates correspond to a parallel memory element is inconsistent with the plain meaning of the term memory in the context of a computer device

because the NAND gates function to pass through signals and not to store signals for later retrieval.

For at least these reasons, Appellant submits that the rejection of claims 1-10 fails and should be reversed.

2. Kanazashi does not disclose exchange of data between clock domains.

Appellant further asserts that Kanazashi does not anticipate Appellant's claims because the input circuit 1 shown in Kanazashi's Figure 5 is not taught as exchanging data between clock domains, but rather as converting input serial data to parallel data for output on a data bus. Appellant's claims recite a device for exchanging data signals between a first clock domain and a second clock domain, along with elements of such device including a parallel memory element coupled to a serial memory element. Appellant submits that the function of exchanging data signals between clock domains is not merely an incidental function, but must bear some relationship to the device elements recited in the claims. The Examiner has provided no such correspondence between the identified elements of Kanazashi's Figure 5 and the function of exchanging data signals between clock domains. The Examiner merely observes that Kanazashi discloses both an internal clock and an external clock, disregarding Kanazashi's teachings that input circuit 1 (which wholly includes the shift register and logic gates alleged to correspond to Appellant's serial and parallel memory elements) is entirely regulated by internal clock CLK1 without transfer to another clock domain (*see, e.g.,* Figure 5 and 6A; Col. 4:40-43).

For these additional reasons, Appellant submits that the rejection of claims 1-10 fails and should be reversed.

3. Kanazashi does not disclose operation of serial and parallel memory elements in different clock domains.

Appellant further submits that Kanazashi cannot be said to anticipate claims 3 and 5 because Kanazashi does not teach or suggest exchanging data between serial and parallel memory elements residing in different clock domains. As discussed above, the cited portions

of Kanazashi do not teach or suggest the recited parallel memory element or the claimed manner of exchanging data between clock domains. Moreover, Appellant finds nothing in Kanazashi to teach or suggest serial and parallel memory elements operating in different clock domains. For example, there is no mention of Kanazashi's external clock (cited by the Examiner) being used for reading the input data from a parallel memory element. Thus, the cited portions of Kanazashi do not teach transferring data between serial and parallel memory elements that reside in different clock domains as in the claimed invention.

For these additional reasons, Appellant submits that the rejection of claims 3 and 5 fails and should be reversed.

4. Kanazashi does not disclose a parallel memory element arranged for writing data signals to be read by a serial memory element.

Appellant further submits that Kanazashi cannot be said to anticipate claim 4 because Kanazashi does not teach or suggest a parallel memory element arranged for writing data signals to be read by a serial memory element. As discussed above, the cited portions of Kanazashi do not teach or suggest the recited parallel memory element. Moreover, Kanazashi's Figure 5 shows an input circuit in which a shift register receives and writes data, the shift register interpreted by the Examiner as corresponding to a serial memory element. Appellant finds nothing in Kanazashi to teach that data is written by a parallel memory element.

For these additional reasons, Appellant submits that the rejection of claim 4 fails and should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejection of claims 1-10 is improper because Kanazashi fails to disclose all the recited claim elements. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/532,294)

1. A device for exchanging data signals between a first clock domain and a second clock domain, characterized in that the device comprises a serial memory element in which successive data elements are shifted in order from one memory location to a next successive memory location, and a parallel memory element coupled to the serial memory element, the serial memory element comprising at least one memory location more for the data signals than the parallel memory element.

2. A device as claimed in claim 1, characterized in that the serial memory element is arranged for writing the data signals and the parallel memory element is arranged for reading out the data signals.

3. A device as claimed in claim 2, characterized in that a first control signal for writing the data signals in the serial memory element can be derived from a first clock signal which is arranged for synchronizing the data signals in the first clock domain, and in that a second control signal for reading the data signals from the parallel memory element can be derived from a second clock signal which is arranged for synchronizing the data signals in the second clock domain.

4. A device as claimed in claim 1, characterized in that the serial memory element is arranged for reading out the data signals and in that the parallel memory element is arranged for writing the data signals.

5. A device as claimed in claim 4 characterized in that a third control signal for reading the data signals from the serial memory element can be derived from a first clock signal which is arranged for synchronizing the data signals in the first clock domain, and in that a fourth control signal for writing the data signals in the parallel memory element can be derived from a second clock signal which is arranged for synchronizing data signals in the second clock

domain.

6. A device as claimed in claim 1, characterized in that the device is arranged for adapting a sample rate of the data signals.

7. A device as claimed in claim 1, characterized in that the device is arranged for changing a modulation scheme of the data signals.

8. A device as claimed in claim 1, characterized in that the data signals are audio samples.

9. A module for transferring data signals between a first and a second clock domain, comprising a device as defined in claim 1.

10. A device for transferring data signals between a first and a second clock domain, comprising a module as claimed in claim 9.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.